UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/023,170	02/13/98	HOLMAN T	042390.P5346

TM02/0215

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BLVD
SEVENTH FLOOR
LOS ANGELES CA 90025-1026

EXAMINER	
VERBRUGGE, K	
ART UNIT	**PAPER NUMBER**
2185	18

DATE MAILED: 02/15/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

See attached Examiner's Answer.

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
ASSISTANT SECRETARY AND COMMISSIONER OF
PATENTS AND TRADEMARKS
Washington, D.C. 20231

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 18

Application Number: 09/023170
Filing Date: 2/13/98
Appellant(s): Thomas J. Holman

Sang Hui Michael Kim
For Appellant

EXAMINER'S ANSWER

This is in response to appellant's brief on appeal filed 12/19/00.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

This appeal involves claims 1-20. Claims 1, 4, 7, 9, 10, 15, 16, and 17 have been amended subsequent to the final rejection.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claims 1-20 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

A substantially correct copy of appealed claims 1-20 appears on pages 13-17 of the Appendix to the appellant's brief. The minor errors are as follows:

In claim 1, line 6, "being" should be deleted to be consistent with the Amendment After Final filed 9/27/00.

In claim 1, line 7, "configured" should be deleted to be consistent with the Amendment After Final filed 9/27/00.

9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal: 4,045,781 LEVY ET AL. 8-1977

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6, 8, 9, 13, and 15-20 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 4,045,781 to Levy et al., hereinafter simply Levy.

Regarding claims 1 and 17-20, Levy shows the claimed system memory controller as memory management unit 22 in Fig. 1, coupled to memory bus 40 through associative memory 24. This system memory controller handles reads and writes as claimed.

Levy shows the claimed memory module as memory module 30 in Fig. 1. Memory module 30 includes the claimed plurality of memory devices as low stack 0-3 and high stack 0-3. Furthermore, memory module 30 includes the claimed memory module controller as memory transceiver 41 and memory control and timing unit 42. This controller receives a first

memory transaction in a first format from the system memory controller and converts it into a second memory transaction in a second format for the plurality of memory devices as claimed. The second memory transaction is clearly different from the first memory format since the outputs of memory transceiver 41 and memory control and timing unit 42 are clearly different from their inputs. This is indicated by the differing nature of the signal lines shown in Fig. 1 and by the other figures (specifically Fig. 11, which details memory control and timing unit 42) and the disclosure (specifically column 6, line 1 through column 9, line 68 and column 16, line 1 through column 17, line 44).

Regarding claim 2, Levy shows the claimed first memory bus as memory bus 40.

Regarding claim 3, Levy does not explicitly show the claimed clock signal line, however his control lines (indicated with "C" in Fig. 1) inherently include such a clock signal line since it is essential for the processor system to be able to regulate its associated memory module(s).

Regarding claim 4, Levy does not explicitly mention the claimed handshake signal line, however it is inherent in his device since his memory controller necessarily communicates data to the system memory controller (memory management unit 22). It is clear that the memory

module controller communicates data and control signals to the system memory controller since the data (D) and control (C) lines of memory bus 40 are bidirectional.

Regarding claim 5, Levy shows the claimed second memory bus as the signal lines coming out of memory transceiver 41 and memory control and timing unit 42.

Regarding claim 6, Levy's second memory bus includes the claimed signal line for a clock signal (timing signal) as shown in Fig. 1.

Regarding claim 8, Levy's memory buses clearly have different numbers of signal lines as shown by Fig. 1.

Regarding claim 9, Levy shows the claimed request handling circuitry as memory transceiver 41 and shows the claimed control logic as memory control and timing unit 42.

Regarding claim 13, Levy teaches that his memory devices are volatile, as claimed, since they are traditional random access memory devices.

Regarding claim 15, Levy shows a second memory module 31 in Fig. 1 which contains the claimed second plurality of memory devices and a second memory module controller as claimed.

Regarding claim 16, since the second plurality of memory devices refer to different memory addresses than the first plurality of memory devices, they store data in a different way than the first plurality of memory devices.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 7, 10, 11, 12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,045,781 to Levy et al., hereinafter simply Levy.

Regarding claim 7, Levy does not teach that his memory buses operate at different rates, however it would have been obvious to one skilled in the art at the time of the invention

to operate them at different rates since they carry different signals and have different lengths, virtually ensuring that the maximum data rate of each one would be different.

Regarding claim 10, Levy shows separate address and data lines for both his first and second memory buses. He does not teach that his first memory bus carries time-multiplexed data and address information as claimed, however it would have been obvious to one skilled in the art to time-multiplex the first address bus to save signal lines and their associated cost and space.

Regarding claims 11, 12, and 14, Levy does not teach that his memory modules have the claimed characteristics, however it would have been obvious to the skilled artisan at the time of the invention to implement Levy's memory modules as SIMMs, DIMMs, or nonvolatile memory devices, as appropriate, depending on design considerations, since all three types of devices were well-known to the artisan.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438,

164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1-20 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of copending Application No. 09/023172 and claims 1-17 of copending Application No. 09/023234. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons.

Claims 1-20 of 09/023170 are directed to a memory module having memory devices and a memory module controller. A system memory controller is connected to the memory module controller with a memory bus.

Claims 1-14 of 09/023172 are directed to a memory module having memory devices and a memory module controller. A system memory controller (or a system memory module) is connected to the memory module controller with a memory bus. The memory module controller comprises interface circuitry to receive transactions from the memory bus and further comprises control logic to generate other transactions for the memory devices.

The memory module controller of 09/023170 necessarily includes interface circuitry to receive transactions from the memory bus and further necessarily includes control logic to generate other transactions for the memory devices, therefore 09/023170 is not patentably distinct from 09/023172.

Claims 1-17 of 09/023234 are directed to a memory module having memory devices and a memory module controller.

The memory module of 09/023234 is necessarily connected to a system memory controller of some sort (a special chip or the CPU) with a memory bus, therefore 09/023170 is not patentably distinct from 09/023234.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

(11) Response to Argument

Appellant's only argument is essentially that Levy fails to show a memory module controller that receives a first memory transaction in a first format and converts it into a second (different) memory transaction in a second (different) format for the plurality of memory devices to which the memory module controller is connected.

Levy clearly shows the claimed memory module controller as memory transceiver 41 and memory control and timing 42 in Fig. 1. The only dispute is whether this memory

module controller converts a received first memory transaction having a first format into a second memory transaction having a different format.

Appellant argues that "memory control and timing circuit 42 initiates a memory cycle after receiving BYTE MASK and ADDRESS PARITY signals. As such, the memory and control timing circuit of [sic] 42 of Levy does not teach converting a first memory transaction into a second memory transaction as recited in claim 1" (emphasis preserved, Appellant's Brief, page 10, first full paragraph). This is Appellant's only support for Appellant's only argument.

As an initial matter, it is noted from Fig. 1 that the memory management unit 22 transmits address (A), data (D), and control (C) signals through associative memory 24, onto memory bus 40, and to the memory module controller (memory transceiver 41 and memory control and timing unit 42). From the figure, it is clear that some reformatting of the data occurs in memory transceiver 41 since the data output from memory transceiver 41 is split onto a low bus for low stacks 0-3 and a high bus for high stacks 3-0. Since the figure indicates parallel operation occurs between similarly numbered low and high stacks, it appears that incoming data is reformatted or split and half is stored in a given low stack, and half is stored in a corresponding high stack.

Furthermore, the outputs from memory control and timing unit 42 indicate that some reformatting is taking place therein: a data gating control signal is transmitted to the memory

transceiver 41 and various control and timing signals are output from the memory control and timing unit 42 to each low stack unit and each high stack unit (each memory device).

The fact that the first memory transaction (output by memory management unit 22) has a first format and the second memory transaction (output by the memory module controller comprising the memory transceiver 41 and memory control and timing unit 42) has a different format is further evidenced by the figures which detail the separate units. Fig. 6 is a block diagram of the memory management unit 22 and shows the various signals output from memory management unit 22. Fig. 20 is a diagram of a portion of memory transceiver 41. Fig. 11 is a diagram of memory control and timing unit 42. Simple inspection of these figures, especially Fig. 11 and its associated Figs. 12-17, indicates that the memory transaction received by memory transceiver 41 and memory control and timing unit 42 is not merely passed on to the memory stack devices but is reformatted to meet the intricate timing and control requirements of the individual low and high stack elements.

Levy further discloses the operation of the circuitry shown in the figures in the disclosure, specifically at column 6, line 1 through column 9, line 68 and column 16, line 1 through column 17, line 44. A careful reading of the disclosure reveals that memory control and timing unit 42 does not merely receive BYTE MASK and ADDRESS PARITY signals as asserted by Appellant, but rather that memory transceiver 41 and memory control and timing unit 42 receive a memory transaction in a first format and convert it into a series of address,

data, timing, and control signals to control the operation of the memory devices (low stack 0-3 and high stack 3-0).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Kevin Verbrugge
Patent Examiner
AU 2185

Jack Lane
Primary Examiner
AU 2185
Conferee

Do Yoo
Supervisory Patent Examiner
AU 2187
Conferee

February 13, 2001

Seventh Floor
12400 Wilshire Blvd
Los Angeles CA 90025